

**CLAIMS**

Please **CANCEL** claims 17-20 as follows:

A status of the claims is provided below.

1. (original) A method for manufacturing a semiconductor device, comprising steps of:  
forming a compressively strained SiGe layer on a silicon substrate;  
ion-implanting atoms to form uniformly distributed interstitial dislocation loops in the SiGe layer; and  
annealing to form uniformly distributed misfit dislocations in the SiGe layer.
2. (original) The method of claim 1, wherein the step of forming the SiGe layer comprises a step of epitaxially growing the SiGe layer on the silicon substrate.
3. (original) The method of claim 2, wherein the SiGe layer is formed at a thickness of approximately 100 Å to 10000 Å.
4. (original) The method of claim 1, further comprising a step of forming a tensilely strained silicon layer on the SiGe layer.
5. (original) The method of claim 1, wherein the step of ion-implanting the atoms causes end-of-range damage in the SiGe layer.

6. (original) The method of claim 1, wherein the step of ion-implanting the atoms causes an amorphous layer to be formed in a surface portion of the SiGe layer.

7. (original) The method of claim 1, wherein the atoms are Ge or Si.

8. (original) The method of claim 1, wherein the atoms are ion-implanted at an implantation concentration of approximately  $1 \times 10^{14}$  atoms/cm<sup>2</sup> to  $1 \times 10^{16}$  atoms/cm<sup>2</sup> at implantation energy of approximately 5 KeV to 100 KeV.

9. (original) The method of claim 1, wherein the step of annealing is formed at a temperature of approximately 500° C to 1100° C for approximately 1 second to 30 minutes.

10. (original) The method of claim 1, wherein density of the interstitial dislocation loops is approximately  $1 \times 10^5$  loops/cm<sup>2</sup> to  $1 \times 10^{12}$  loops/cm<sup>2</sup>.

11. (original) The method of claim 10, wherein density of the misfit dislocations is approximately  $1 \times 10^5$  #/cm<sup>2</sup> to  $1 \times 10^{12}$  #/cm<sup>2</sup>.

12. (original) A method for forming a semiconductor substrate, comprising the steps of:

forming a SiGe layer on a silicon substrate, wherein the SiGe layer is compressively strained;

controllably ion-implanting atoms onto the SiGe layer causing uniformly distributed end-of-range damage therein;

annealing to form interstitial dislocation loops uniformly distributed in the SiGe layer, wherein the uniformly distributed interstitial dislocation loops nucleate uniformly distributed misfit dislocations in the SiGe layer; and

forming a tensilely strained silicon layer on the SiGe layer.

13. (original) The method of claim 12, wherein the step of ion-implanting the atoms causes an amorphous layer to be formed in a surface portion of the SiGe layer.

14. (original) The method of claim 12, wherein the atoms are Ge or Si.

15 (original) The method of claim 12, wherein the atoms are ion-implanted at an implantation concentration of approximately  $1 \times 10^{14}$  atoms/cm<sup>2</sup> to  $1 \times 10^{16}$  atoms/cm<sup>2</sup> at implantation energy of approximately 5 KeV to 100 KeV.

16. (original) The method of claim 12, wherein the step of annealing is formed at a temperature of approximately 500° C to 1100° C for approximately 1 second to 30 minutes.

17-20. (canceled)